IN THE CLAIMS:

1. (Currently Amended) An analog switch circuit for sampling an analog input signal, the circuit comprising:

an analog switch section including a first n-channel MOS field effect transistor and a first p-channel MOS field effect transistor, sources of which are connected, drains of which are connected, and therefore ~~which~~ said first n-channel and first p-channel MOS field transistors are connected in parallel, for ~~inputting an~~ receiving the analog input signal and for outputting a sampled analog output signal;

a comparator circuit for ~~inputting~~ receiving the analog input signal and a reference signal and for comparing the input potential of the analog input signal and the reference potential of the reference signal; and

a voltage boost circuit for setting a potential of a gate of the first n-channel MOS field effect transistor to a potential of positive power supply voltage in the case of the input potential of the analog input signal being lower than the reference potential at the time of the analog switch section being in a continuity state and for boosting the potential of the gate to a potential higher than the potential of the positive power supply voltage in the case of the input potential of the analog input signal being higher than the reference potential at the time of the analog switch section being in [[a]] the continuity state.

2. (Currently Amended) The analog switch circuit according to claim 1, wherein the comparator circuit includes a filter for absorbing a drop in the input potential of the analog input signal input at the time of the analog switch section being in [[a]] the continuity state.

3. (Currently Amended) The analog switch circuit according to claim 1, further comprising a signal line for ~~inputting~~ receiving a signal for performing ~~the voltage boost~~ boosting of the potential of the gate of the first n-channel MOS field effect transistor to the potential higher than the potential of the positive power supply voltage regardless of the result of a comparison made by the comparator circuit.

4. (Currently Amended) The analog switch circuit according to claim 1, further comprising a signal line for ~~inputting~~ receiving a signal for not performing ~~the voltage boost~~ boosting of the potential of the gate of the first n-channel MOS field effect transistor to the potential higher than the potential of the positive power supply voltage regardless of the result of a comparison made by the comparator circuit.

5. (Currently Amended) An analog switch circuit for sampling an analog input signal, the circuit comprising:

an analog switch section including a first n-channel MOS field effect transistor and a first p-channel MOS field effect transistor, sources of which are connected, drains of which are connected, and therefore ~~which~~ said first n-channel and first p-channel MOS field effect transistors are connected in parallel, for ~~inputting an~~ receiving the analog input signal and for outputting a sampled analog output signal;

a comparator circuit for ~~inputting~~ receiving the analog input signal and a reference signal and for comparing the input potential of the analog input signal and the reference potential of the reference signal; and

a circuit for setting a potential of a gate of the first p-channel MOS field effect transistor to a potential of negative power supply voltage or ground potential in the case of the input potential of the analog input signal being higher than the reference potential

at the time of the analog switch section being in a continuity state and for setting the potential of the gate to a potential lower than the potential of the negative power supply voltage or the ground potential in the case of the input potential of the analog input signal being lower than the reference potential at the time of the analog switch section being in [[a]] the continuity state.

6. (Currently Amended) The analog switch circuit according to claim 5, wherein the comparator circuit includes a filter for absorbing a rise in the input potential of the analog input signal input at the time of the analog switch section being in [[a]] the continuity state.

7. (Currently Amended) The analog switch circuit according to claim 5, further comprising a signal line for ~~inputting~~ receiving a signal for setting the potential of the gate to the potential lower than the potential of the negative power supply voltage or the ground potential regardless of the result of a comparison made by the comparator circuit.

8. (Currently Amended) The analog switch circuit according to claim 5, further comprising a signal line for ~~inputting~~ receiving a signal for not setting the potential of the gate to the potential lower than the potential of the negative power supply voltage or the ground potential regardless of the result of a comparison made by the comparator circuit.